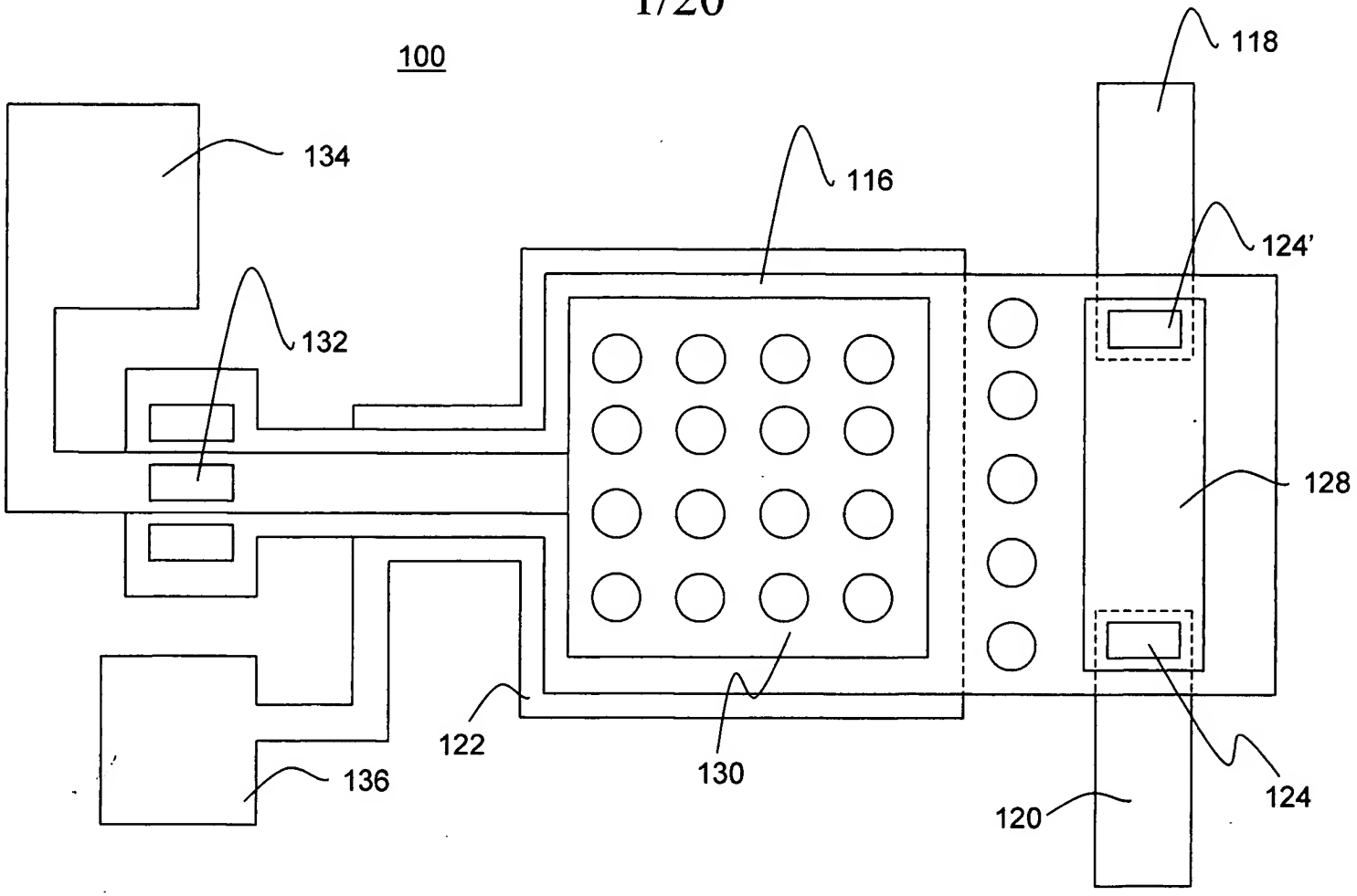

FIG. 1A
PRIOR ART

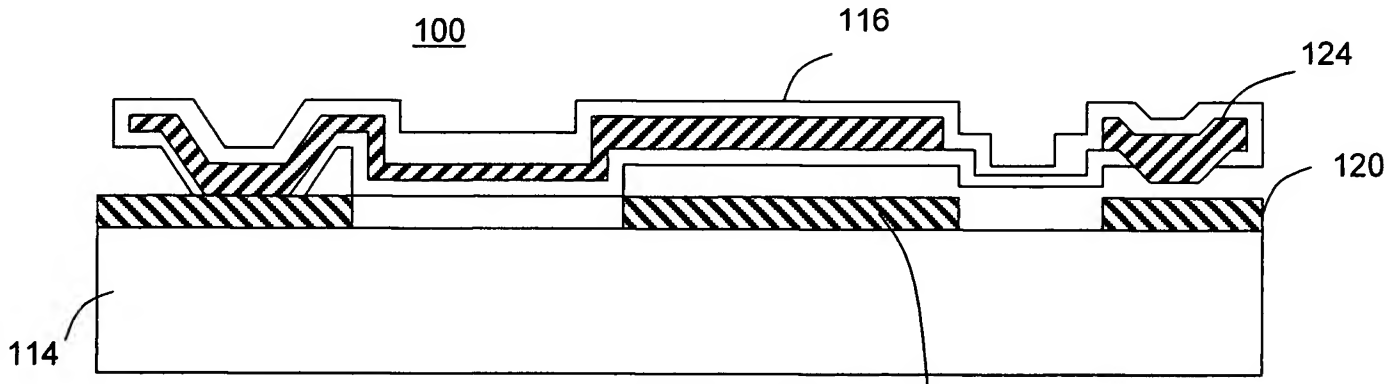

FIG. 1B
PRIOR ART

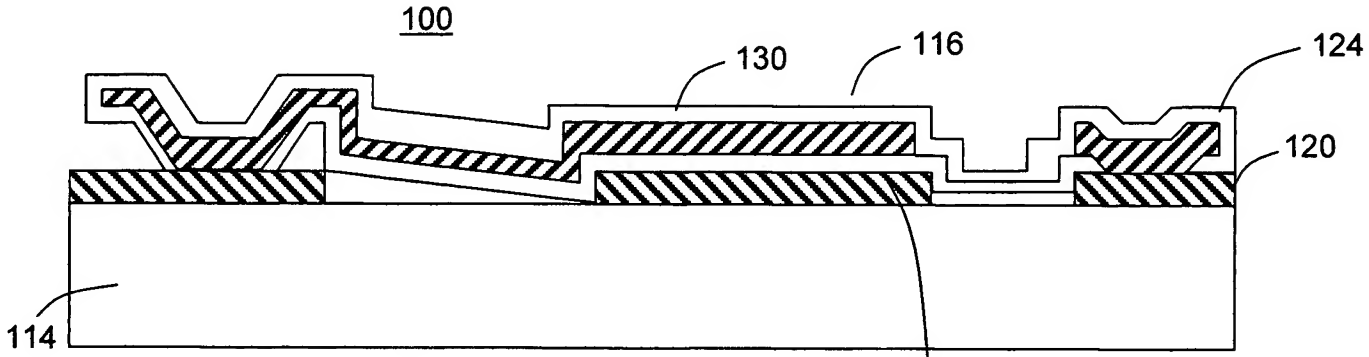

FIG. 1C
PRIOR ART

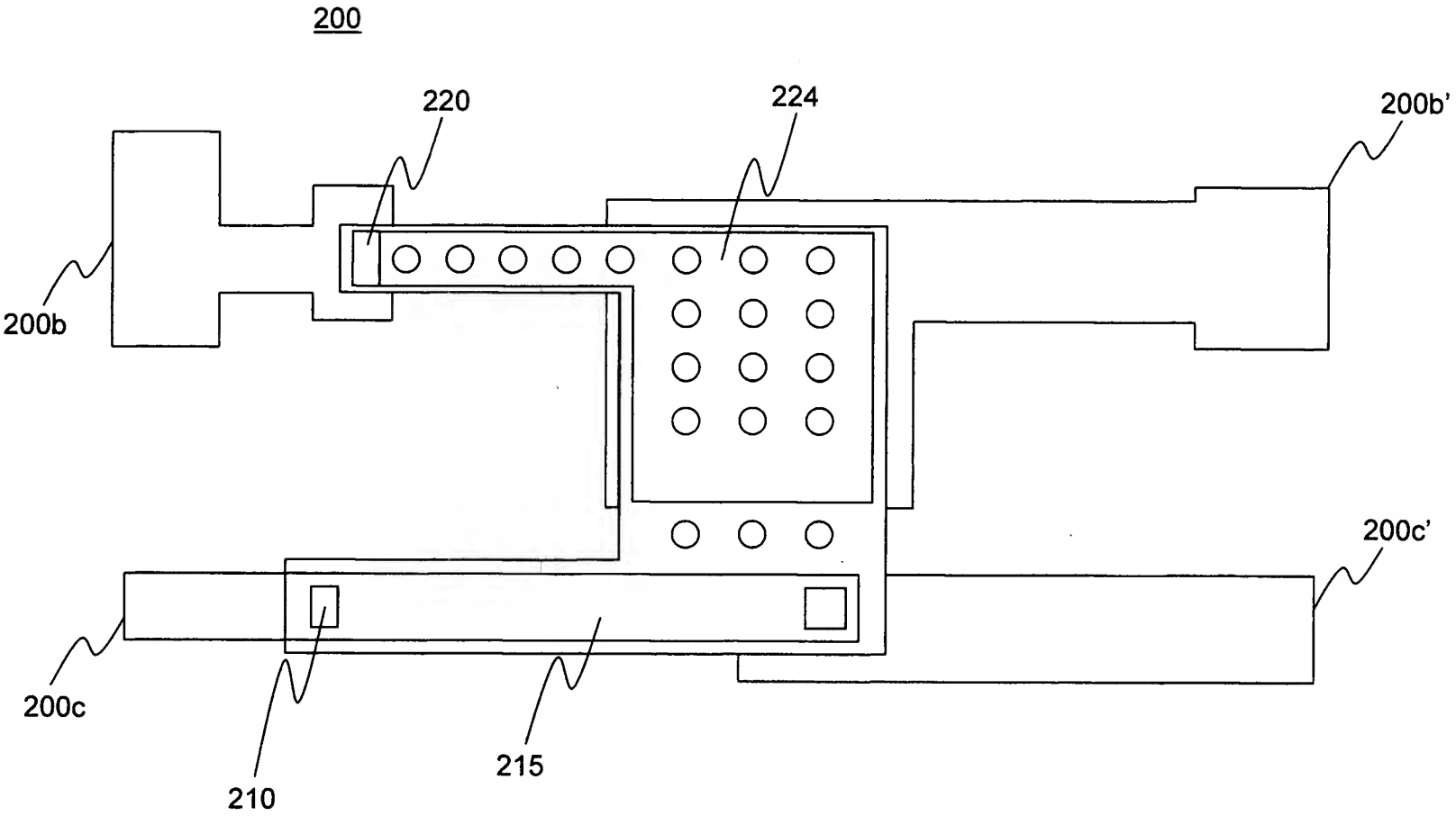

FIG. 2A
PRIOR ART

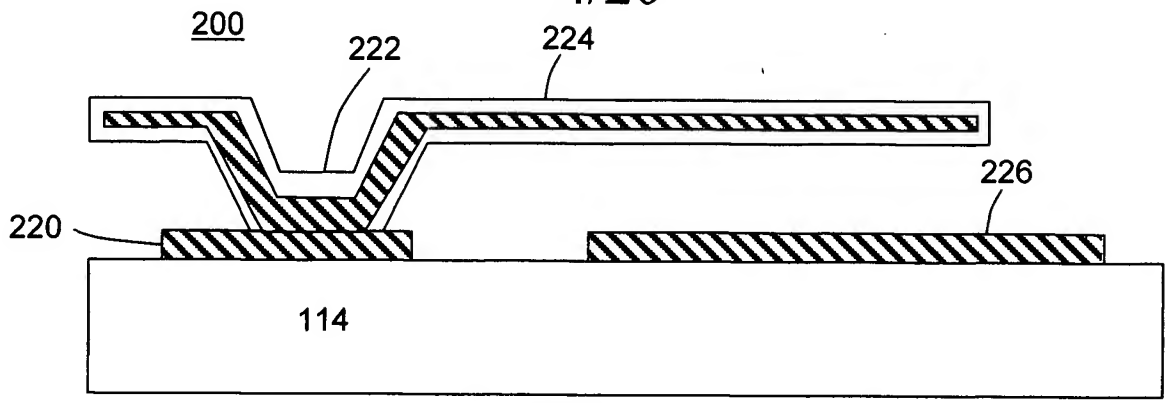

FIG. 2B
PRIOR ART

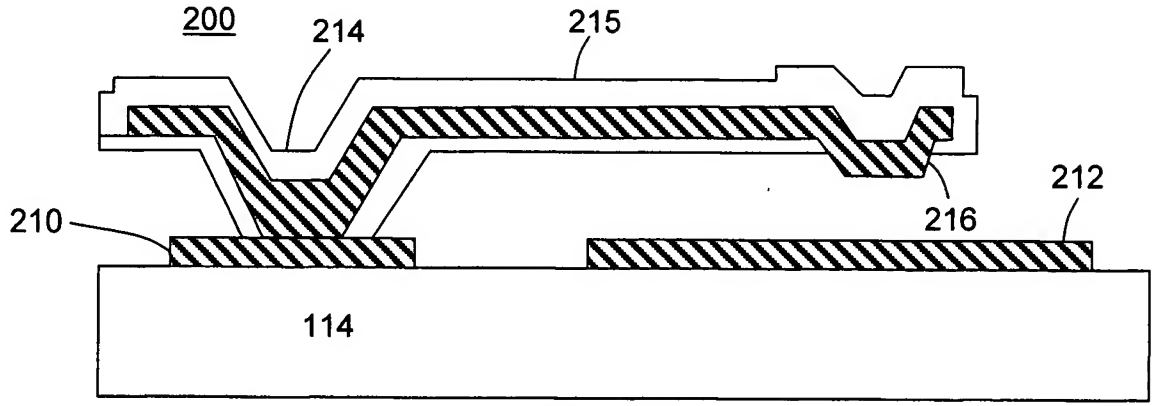

FIG. 2C
PRIOR ART

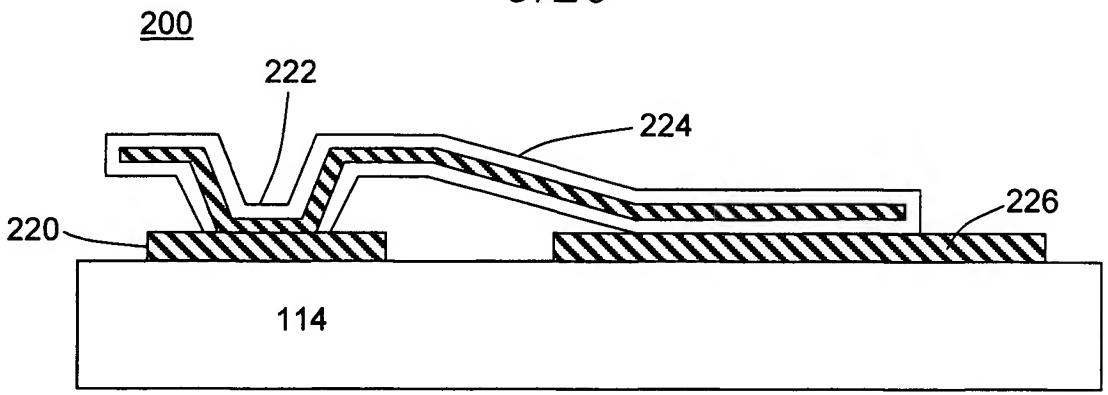

FIG. 2D
PRIOR ART

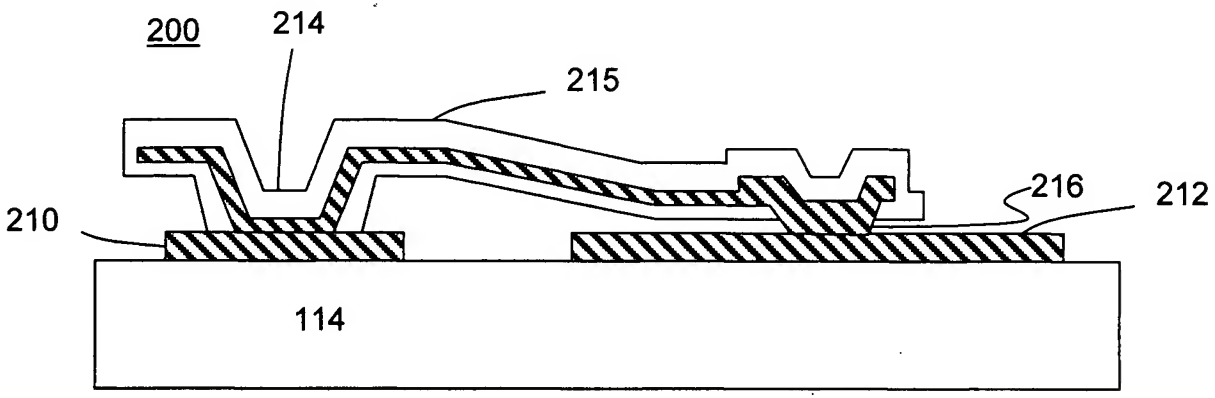

FIG. 2E
PRIOR ART

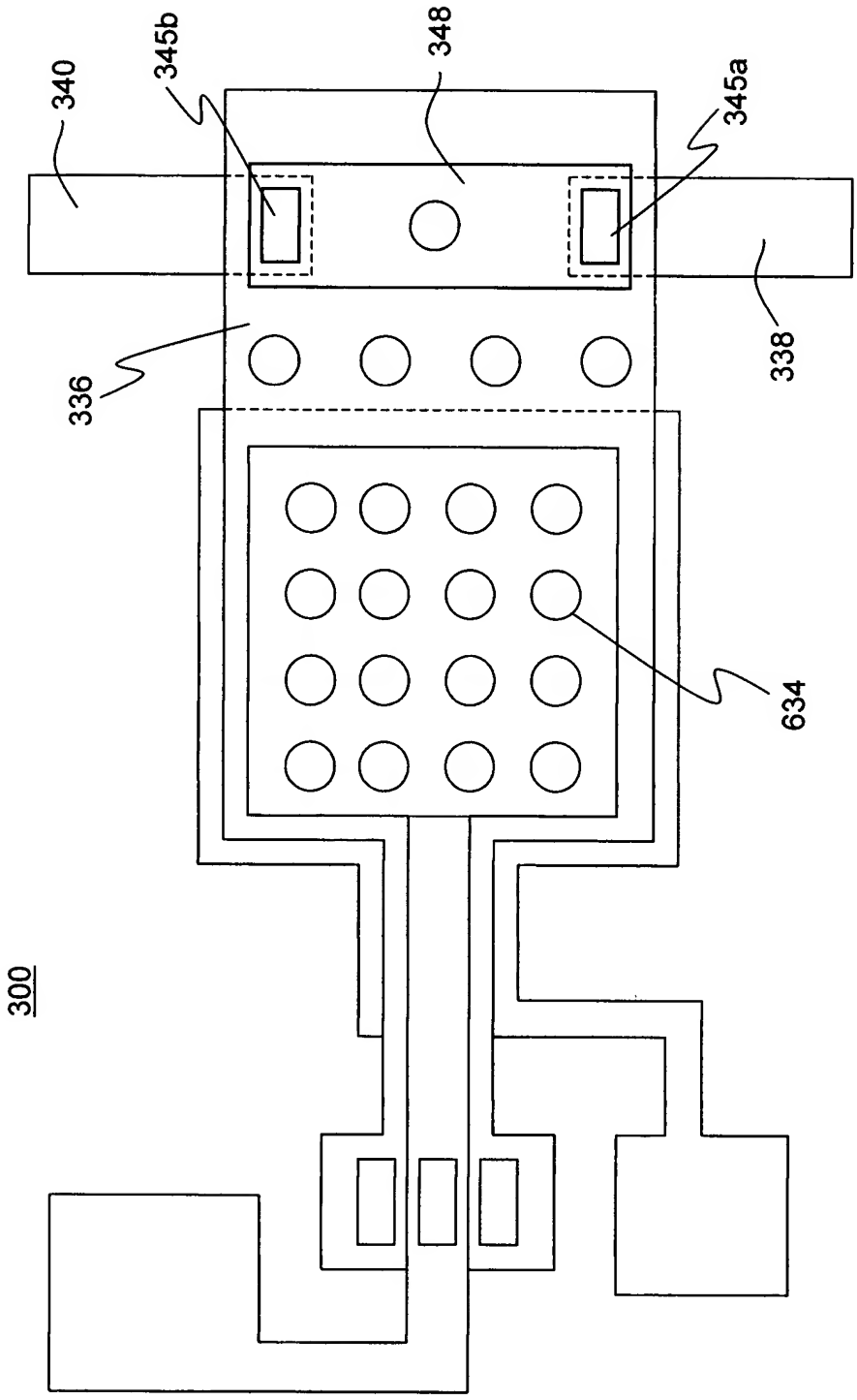

FIG. 3A

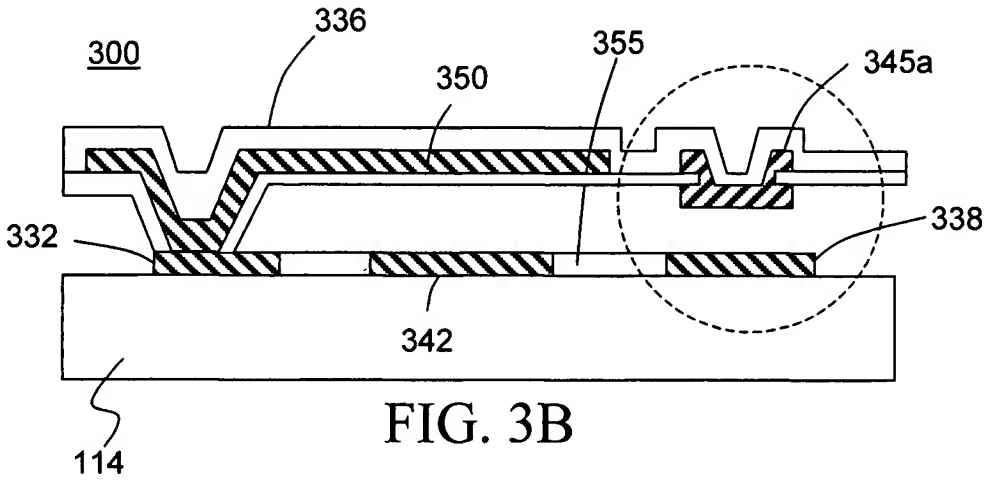

FIG. 3B

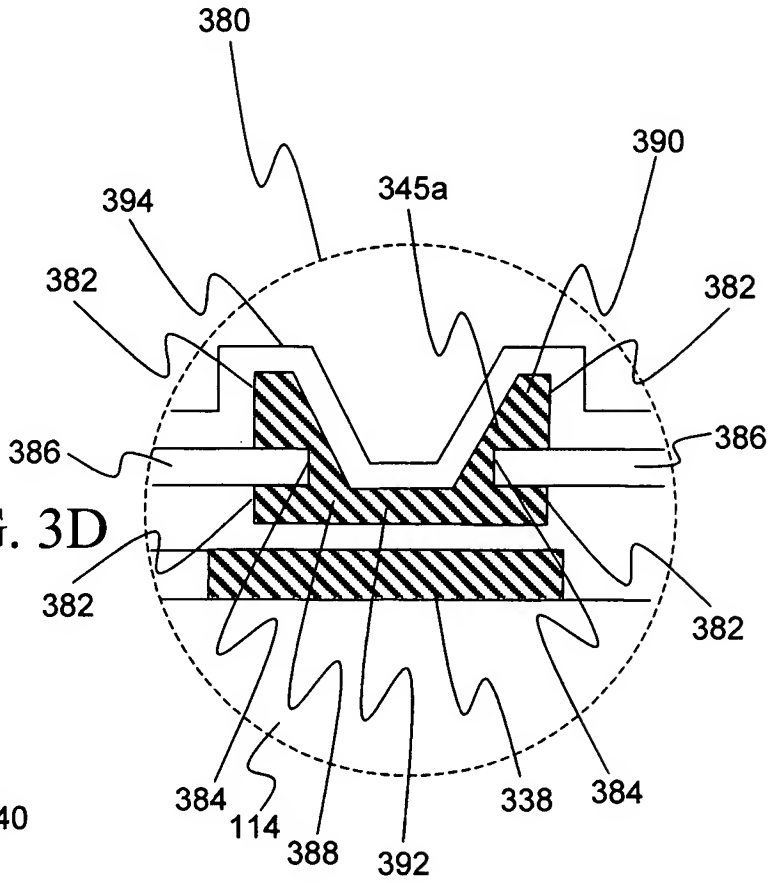

FIG. 3D

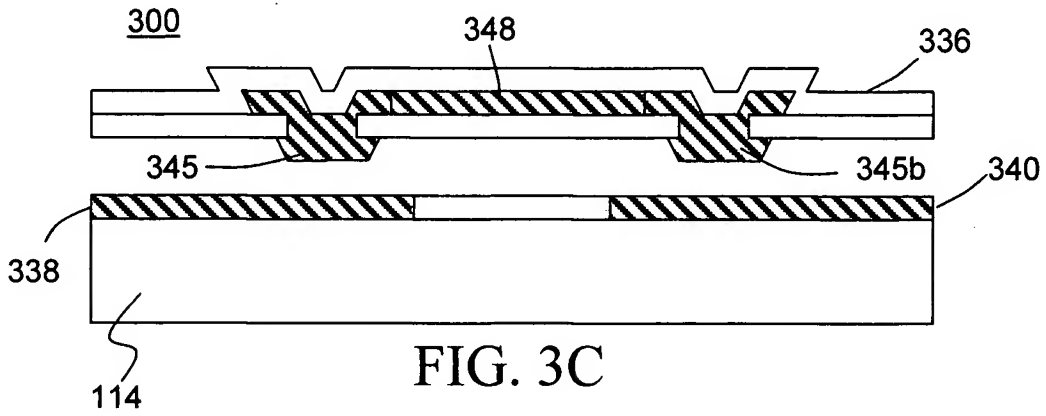

FIG. 3C

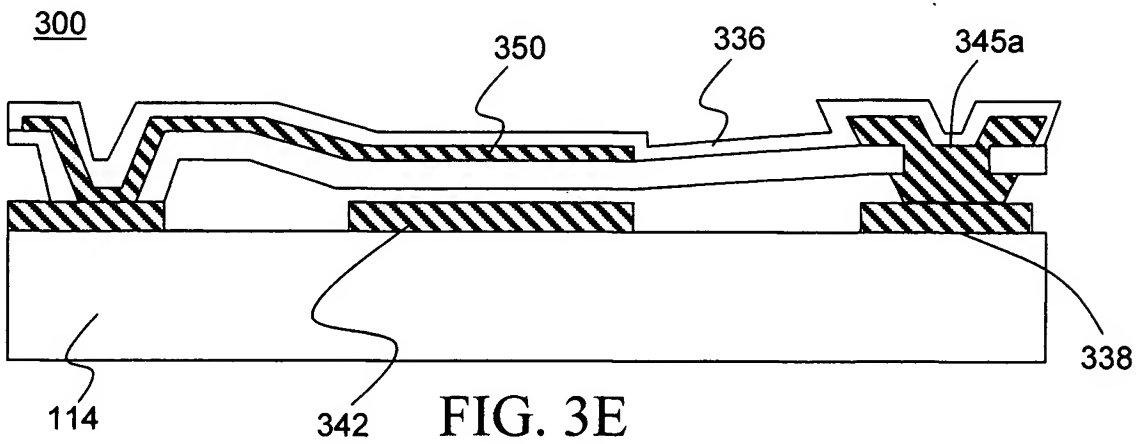

FIG. 3E

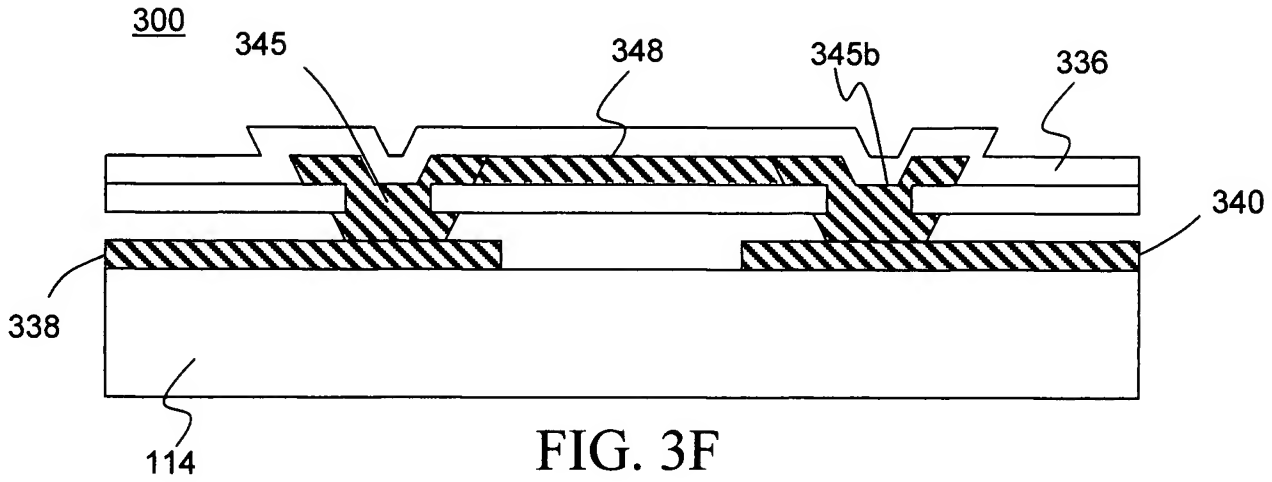

FIG. 3F

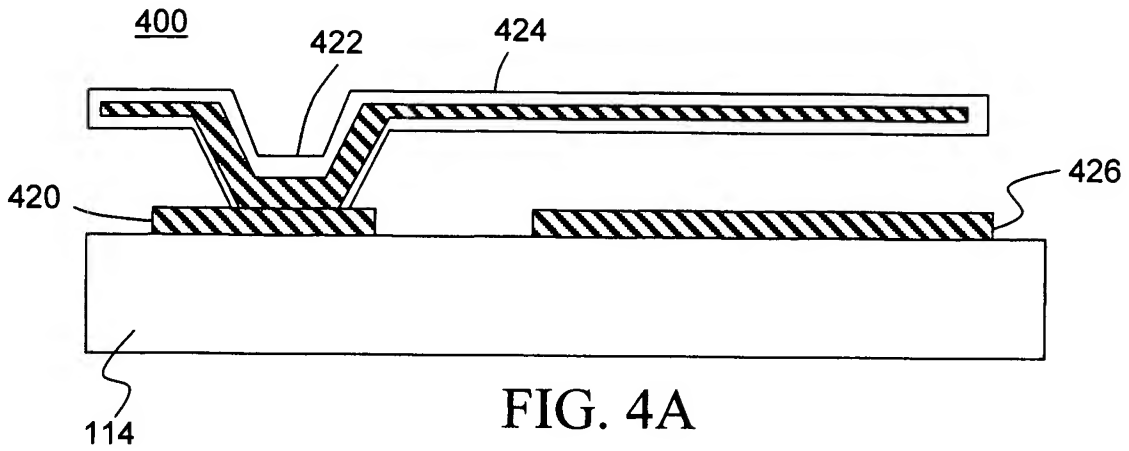

FIG. 4A

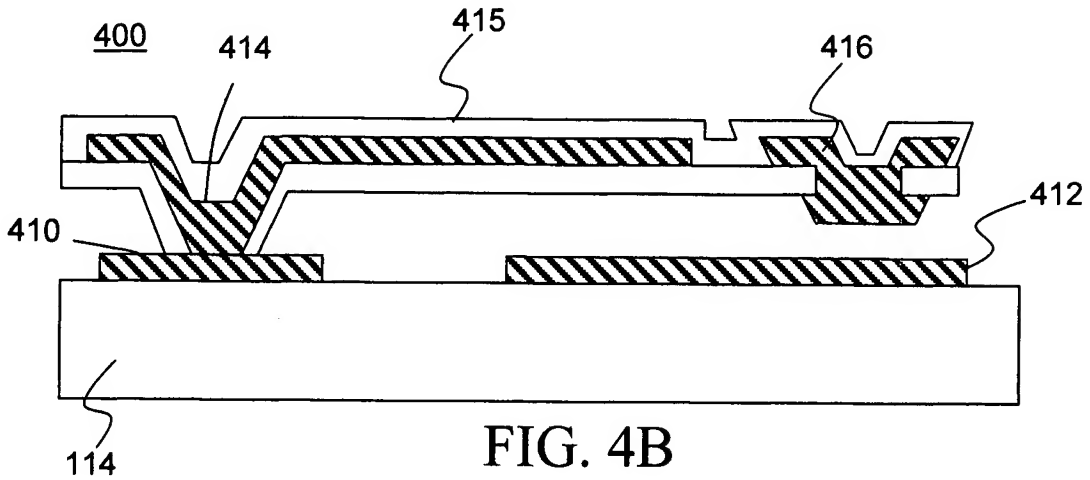

FIG. 4B

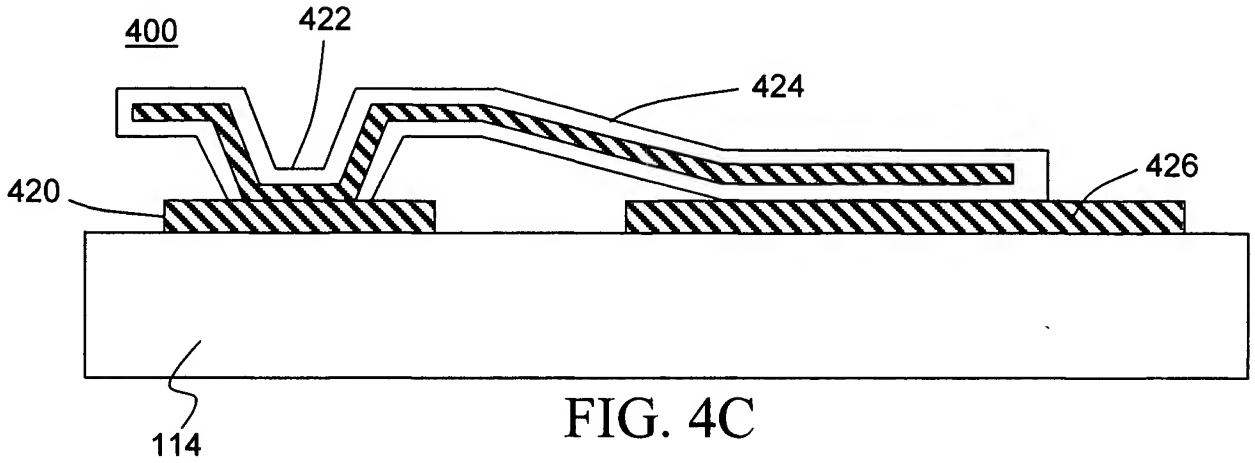

FIG. 4C

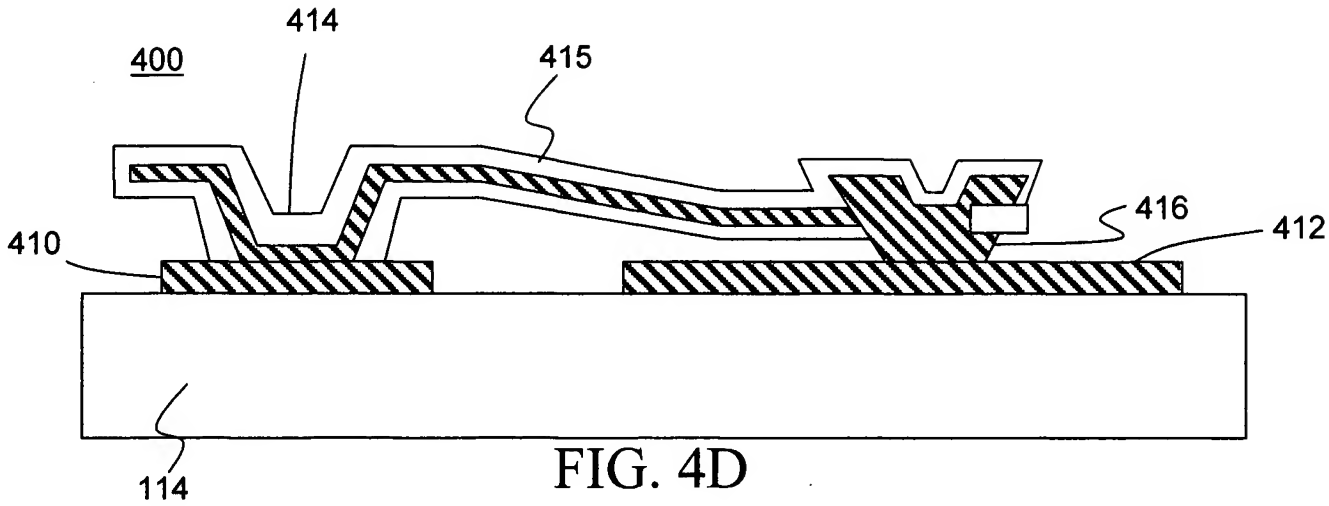

FIG. 4D

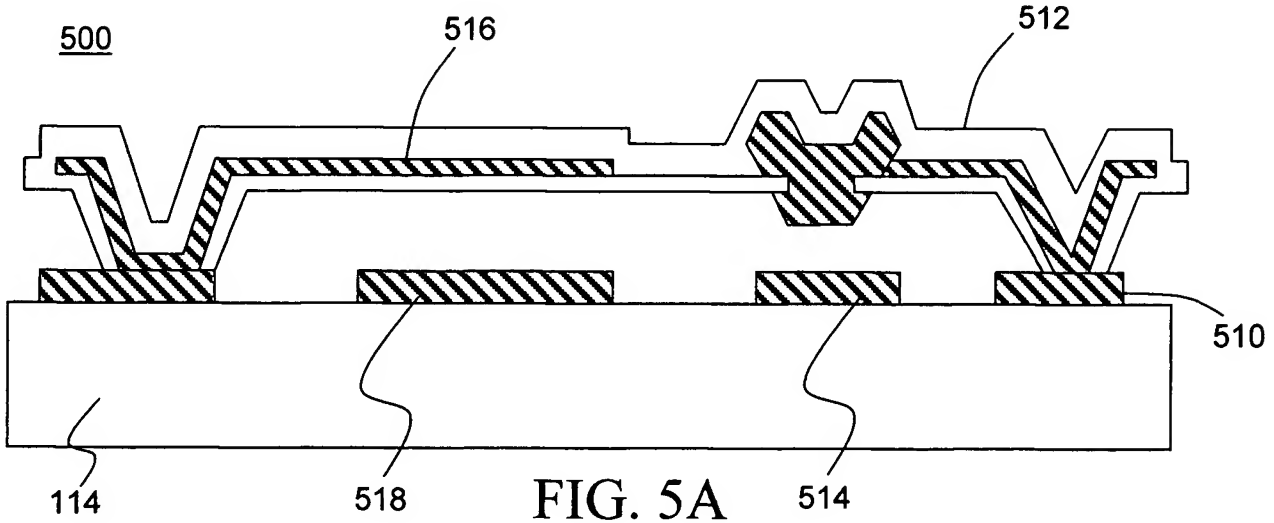

FIG. 5A

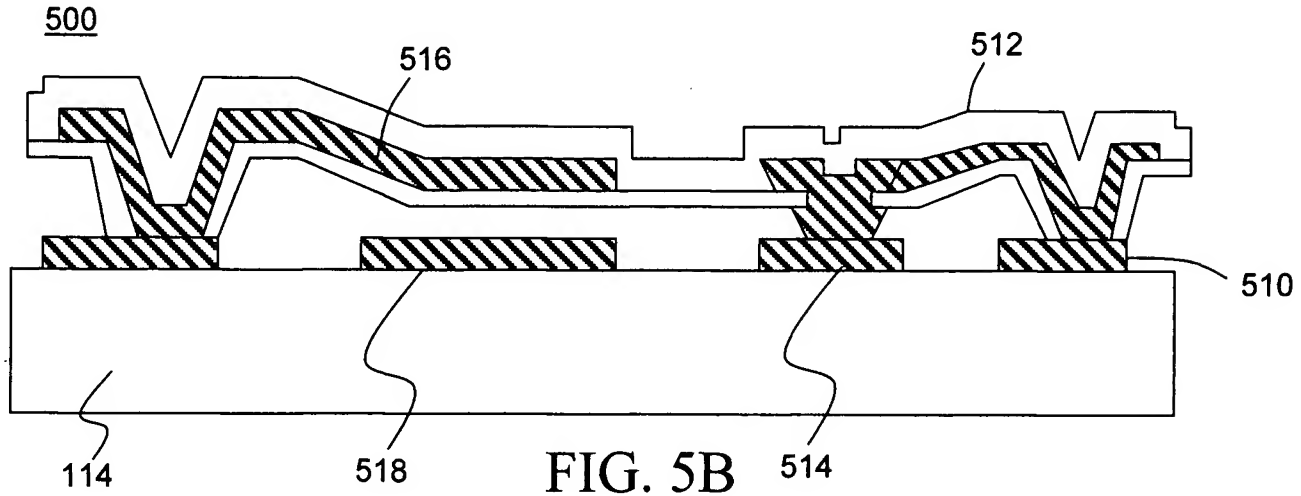

FIG. 5B

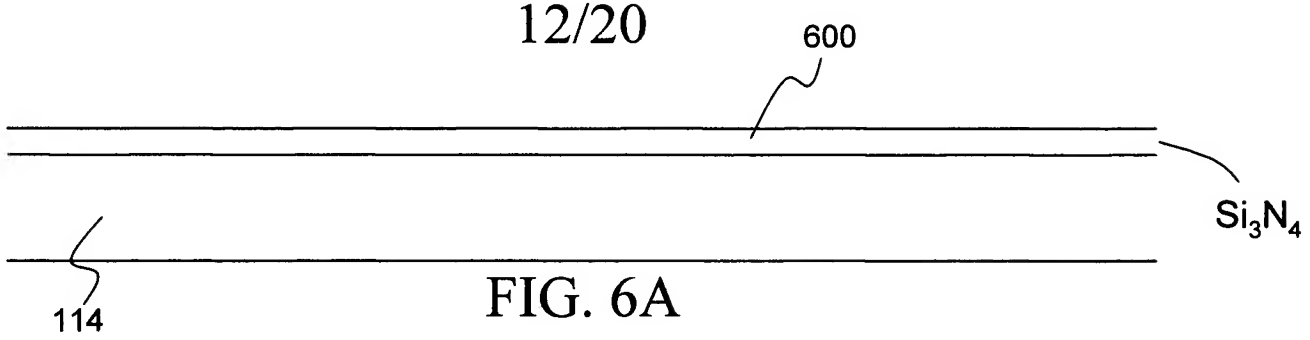

FIG. 6A

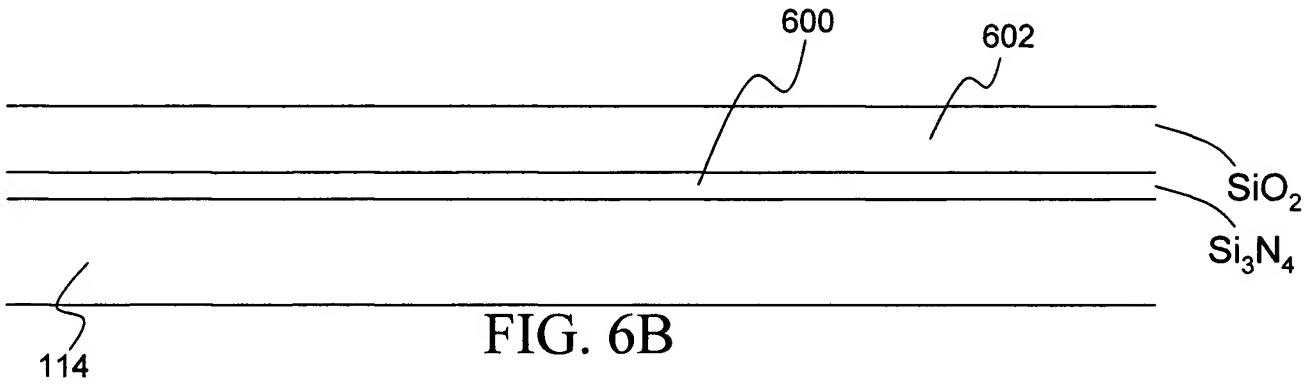

FIG. 6B

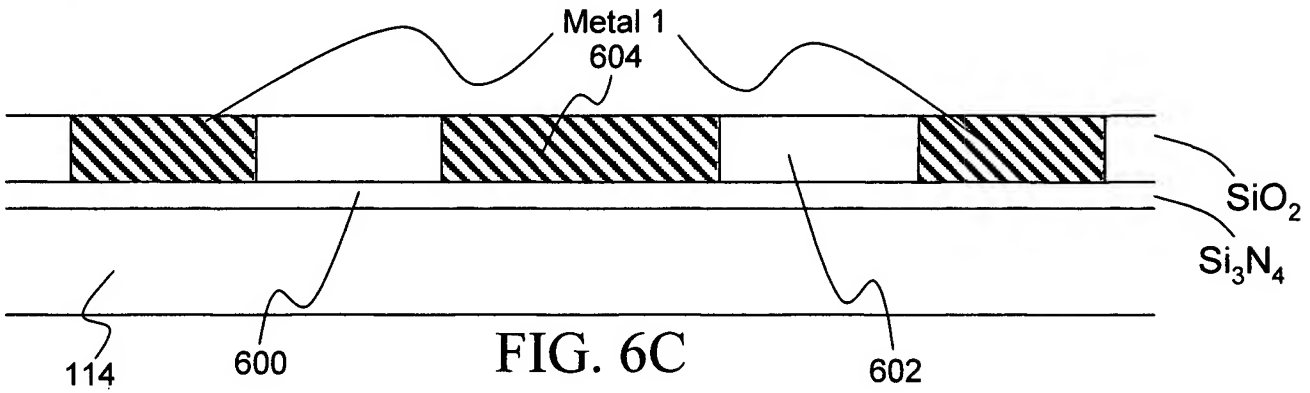

FIG. 6C

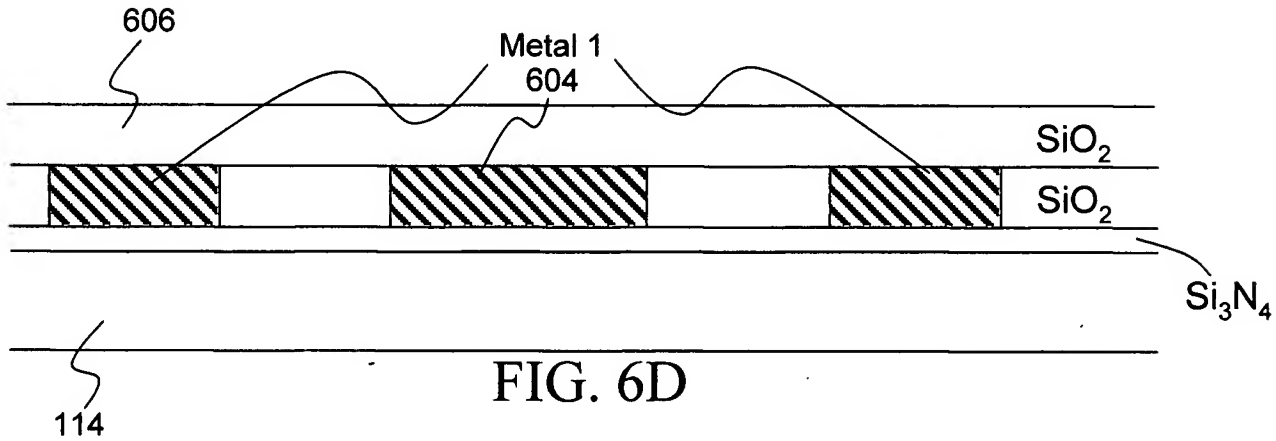
606
Metal 1
604
SiO_2
SiO_2
Si_3N_4
114

FIG. 6D

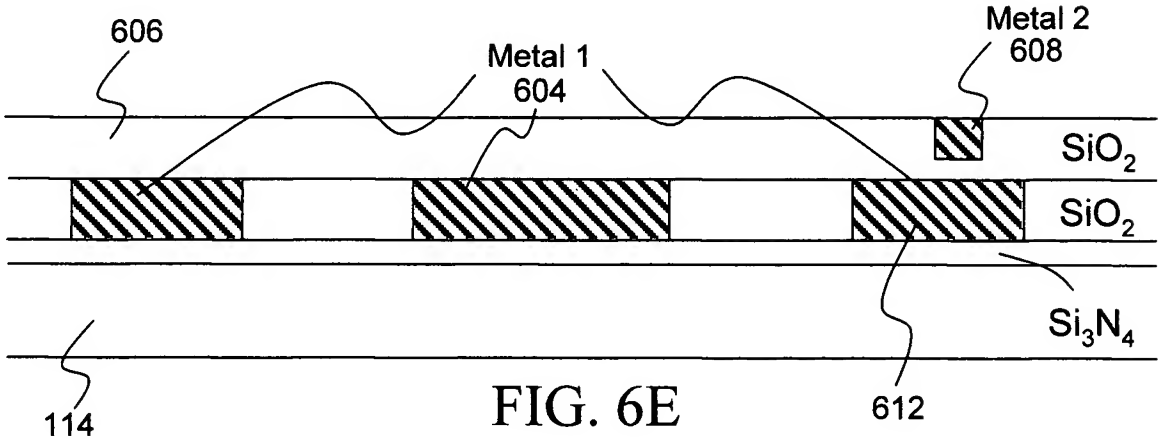
606
Metal 1
604
Metal 2
608
SiO_2
SiO_2
Si_3N_4
114
612

FIG. 6E

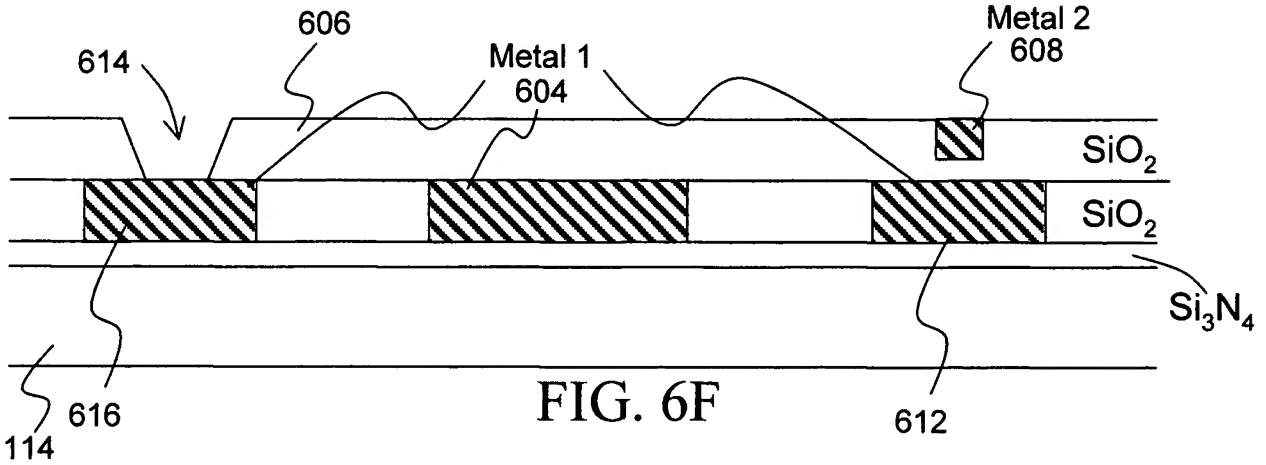
606
614
Metal 1
604
Metal 2
608
SiO_2
SiO_2
Si_3N_4
616
114
612

FIG. 6F

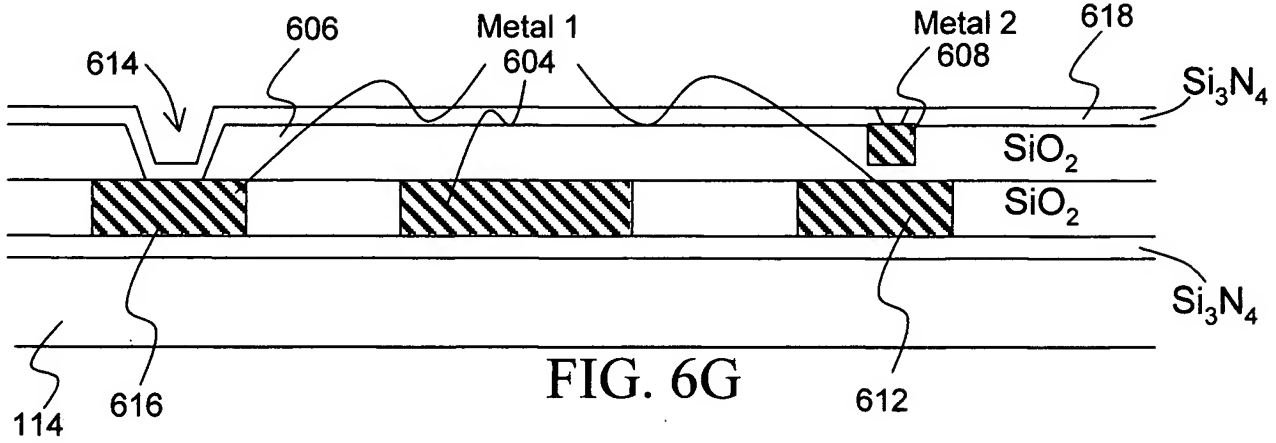
606
Metal 1
604
Metal 2
608
618
614
Si_3N_4
SiO_2
SiO_2
Si_3N_4
616
114
612

FIG. 6G

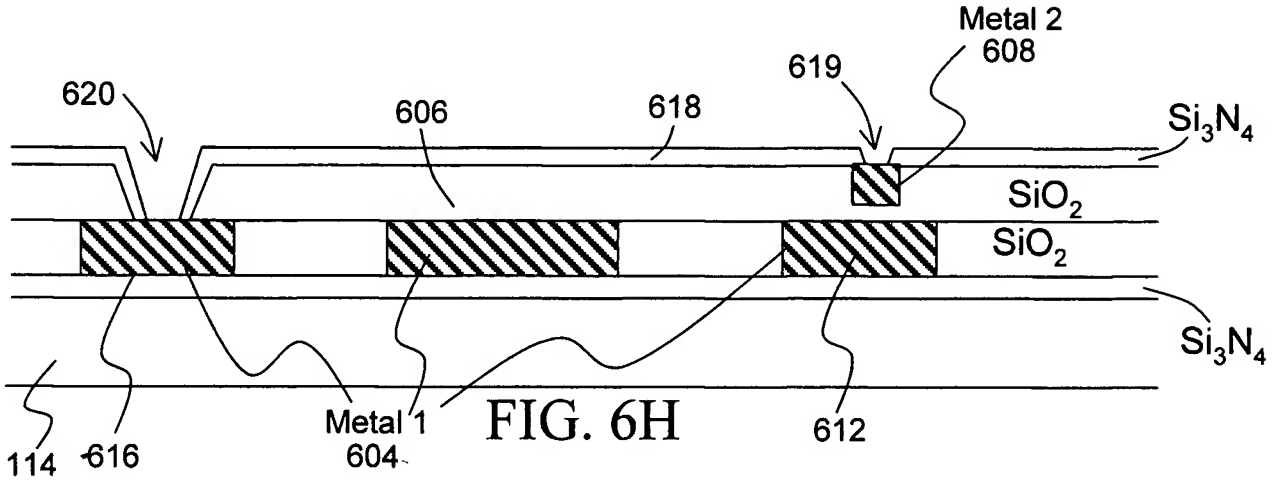
Metal 2
608
619
620
606
618
Si_3N_4
SiO_2
SiO_2
Si_3N_4
114
616
Metal 1
604
612

FIG. 6H

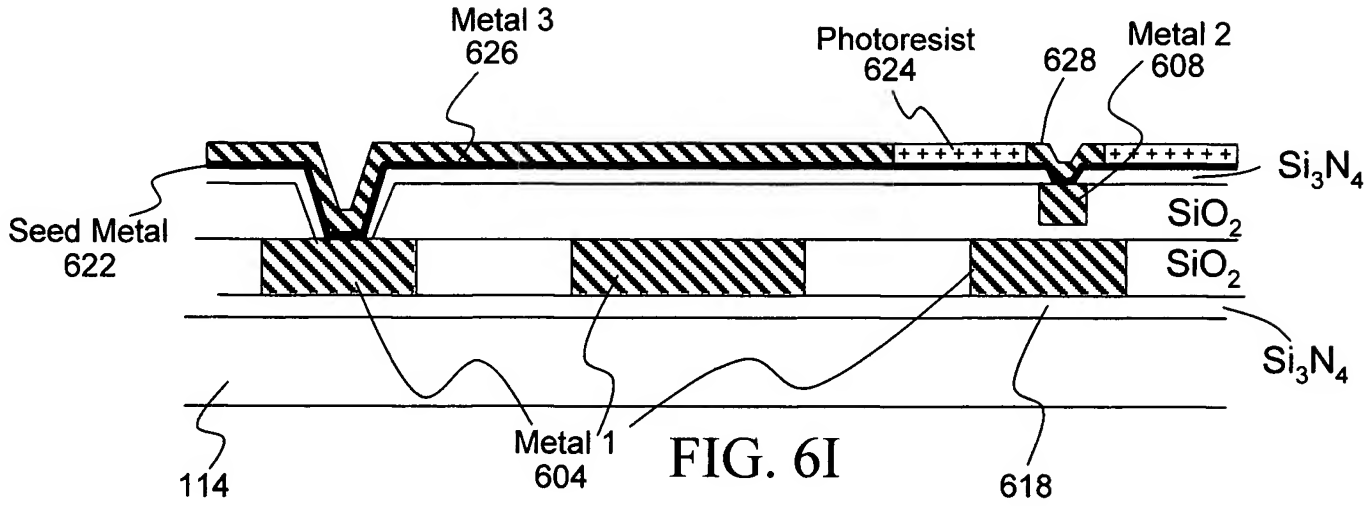
Metal 3
626
Photoresist
624
628
Metal 2
608
Si_3N_4
Seed Metal
622
SiO_2
SiO_2
Si_3N_4
114
Metal 1
604
618

FIG. 6I

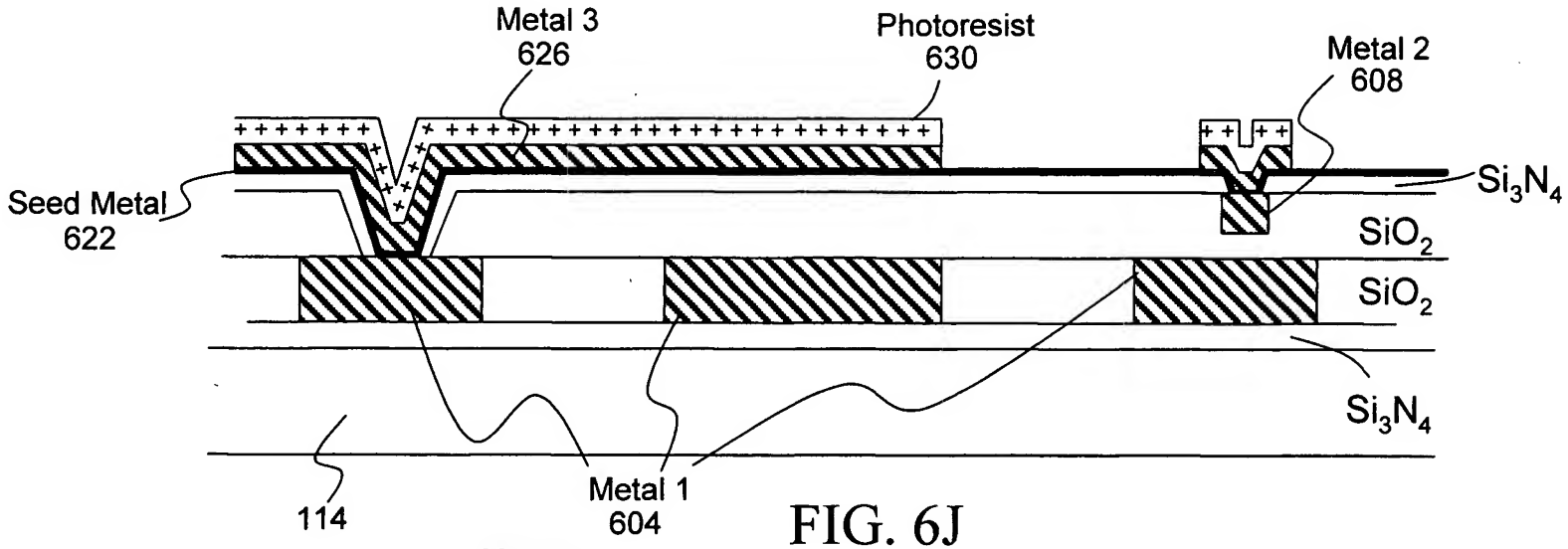
Metal 3
626
Photoresist
630
Metal 2
608
Seed Metal
622
Si_3N_4
SiO_2
SiO_2
Si_3N_4
114
Metal 1
604

FIG. 6J

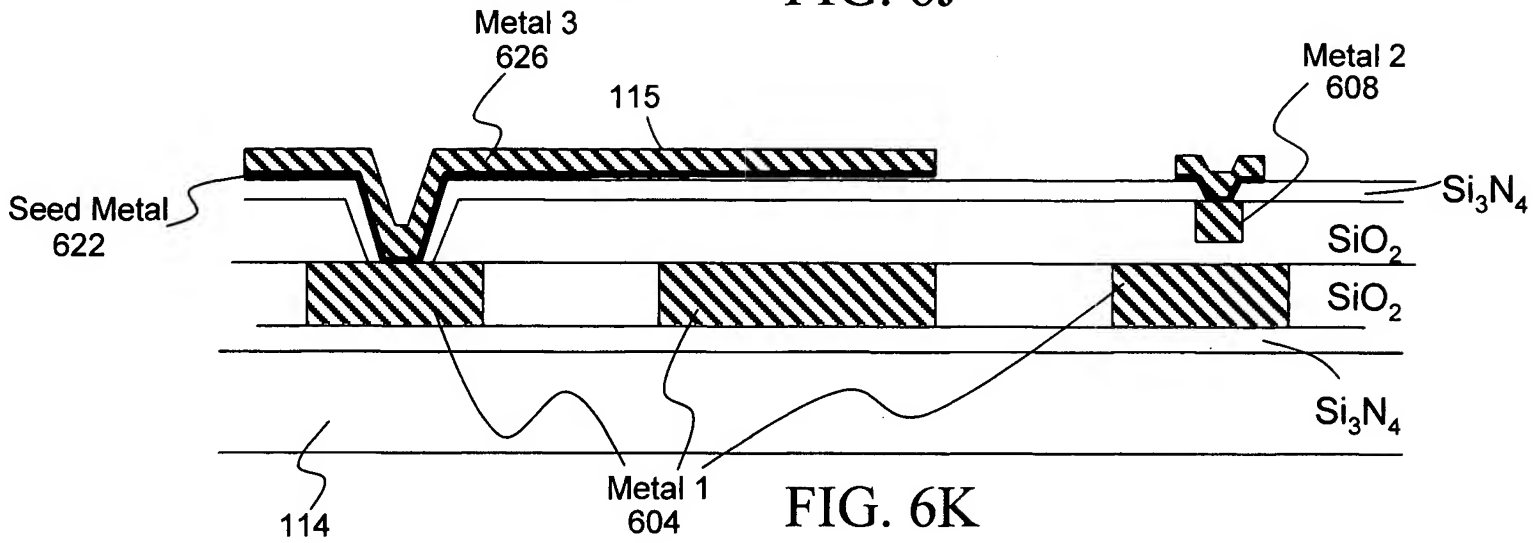
Metal 3
626
115
Metal 2
608
Seed Metal
622
Si_3N_4
SiO_2
SiO_2
Si_3N_4
114
Metal 1
604

FIG. 6K

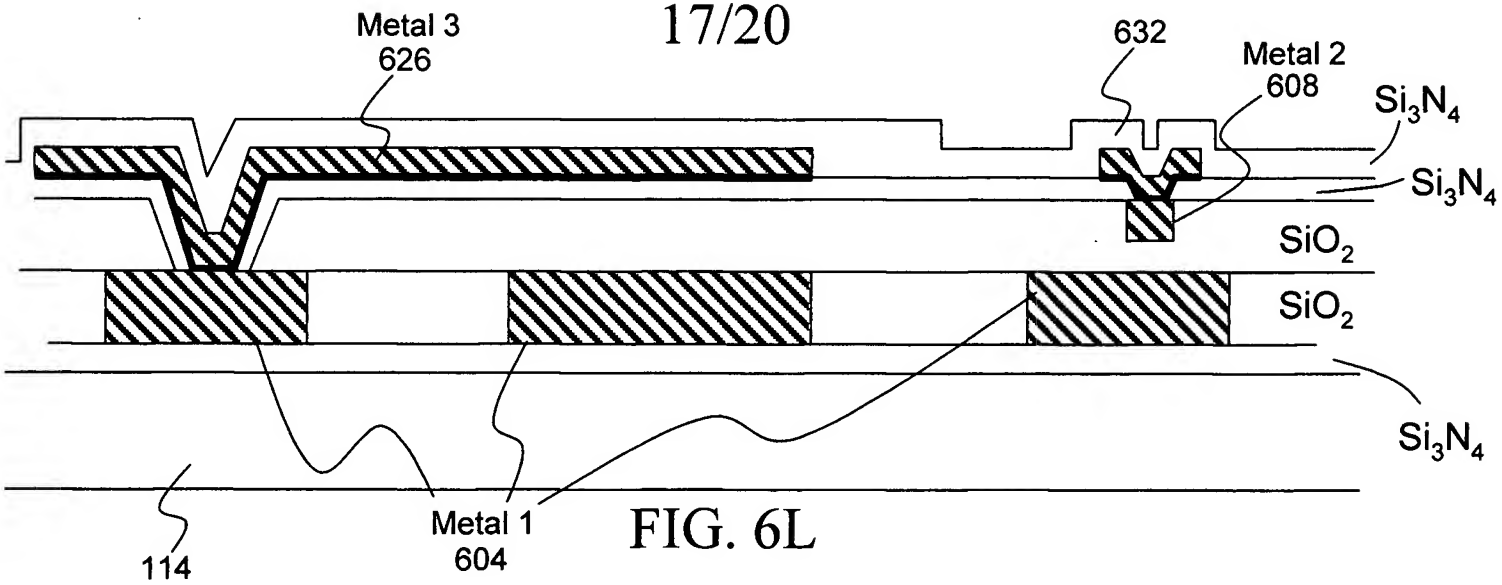
Metal 3
626
632
Metal 2
608
Si_3N_4
Si_3N_4
SiO_2
SiO_2
Si_3N_4
114
Metal 1
604

FIG. 6L

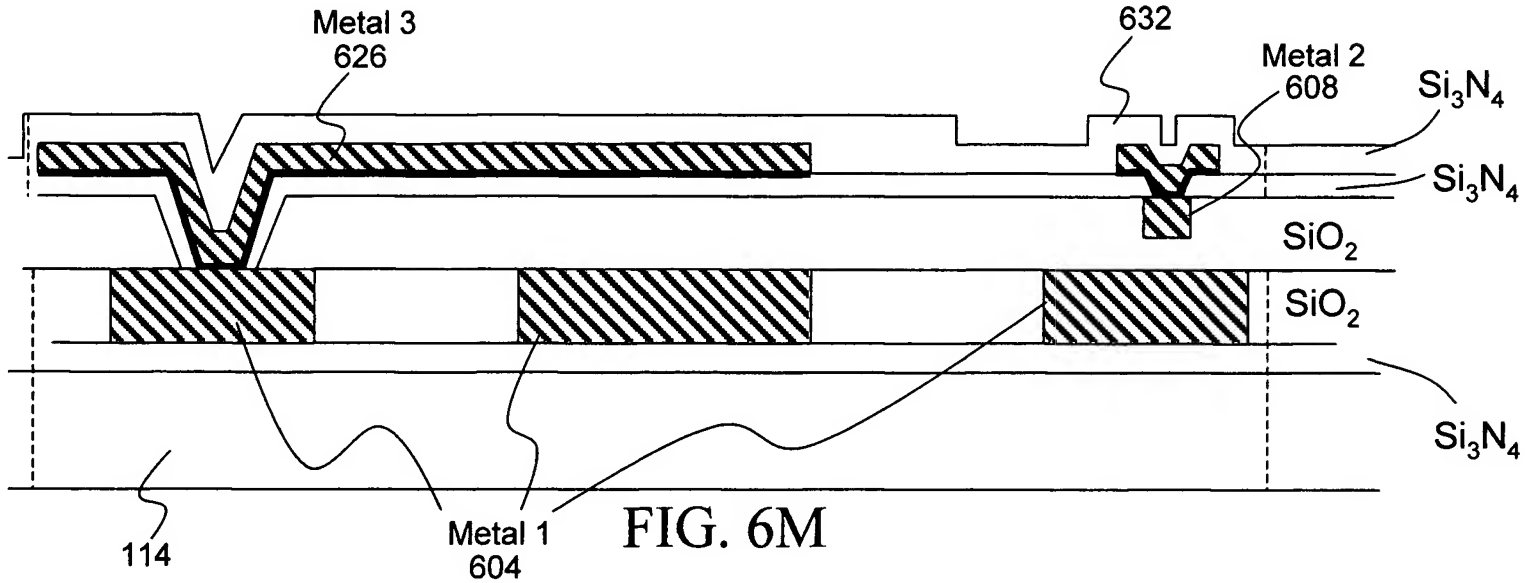
Metal 3
626
632
Metal 2
608
Si_3N_4
Si_3N_4
SiO_2
SiO_2
Si_3N_4
114
Metal 1
604

FIG. 6M

Layer	Materials	Deposit Process	Removal Process	Etch Process	Thickness
Substrate	Semiconducting Insulators, e.g., Silicon, GaAs, Quartz, Sapphire	N/A	N/A	N/A	300 μm - 600 μm
Dielectric Layer	Nitride, Oxide, Phosphorous Doped Oxide	PECVD, LPCVD	N/A	Wet Etch/Dry Etch	.1 μm - 5 μm
Photoresist	Positive Photoresist/Negative Photoresist	Spin Coat	Resist Stripper/Plasma Stripping	Spray Develop/Tank Develop	1 μm-8 μm
Substrate Electrodes	Goal/Any Conductor	E-beam Evaporation, Thermal Evaporation, Sputtering	N/A	Lift-off, Pattern and Etch	.5 μm-5 μm
Sacrificial Layer	Oxide, Silicon Metal (i.e., Al)	PECVD, LPCVD, E-Beam Evaporation	Wet Etch/Dry Etch	N/A	.5 μm-5 μm
1st Insulating Layer	Nitride/Oxide	PECVD	N/A	Dry Etch	.5 μm-5 μm
Top Electrode Layer(s)	Gold/Any Conductor	E-Beam Evaporation, Thermal Evaporation, Plating	N/A	Wet Etch	.5 μm-5 μm
2nd Insulating Structure Layer	Nitride, Oxide	PECVD	N/A	Dry Etch, Ion Milling	.5 μm-5 μm

FIG. 7

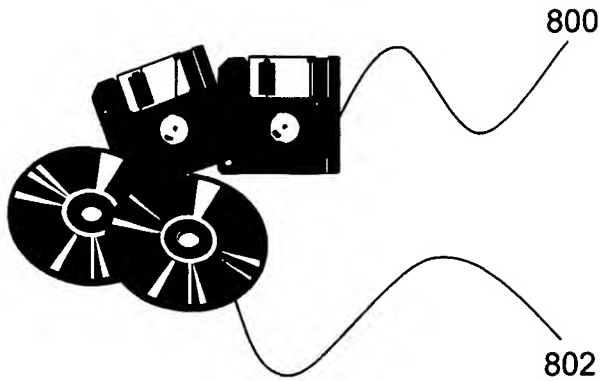

FIG. 8

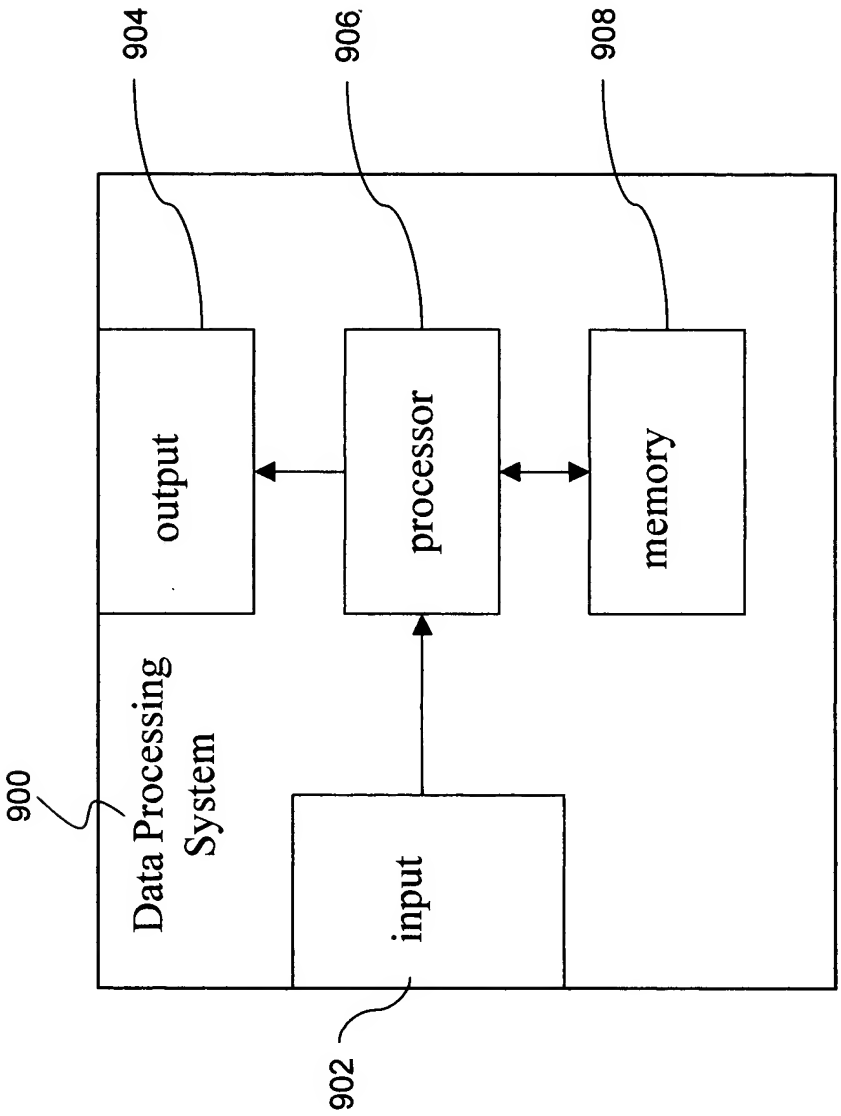
904
906
908
output
processor
memory
Data Processing System
900
input
902

FIG. 9